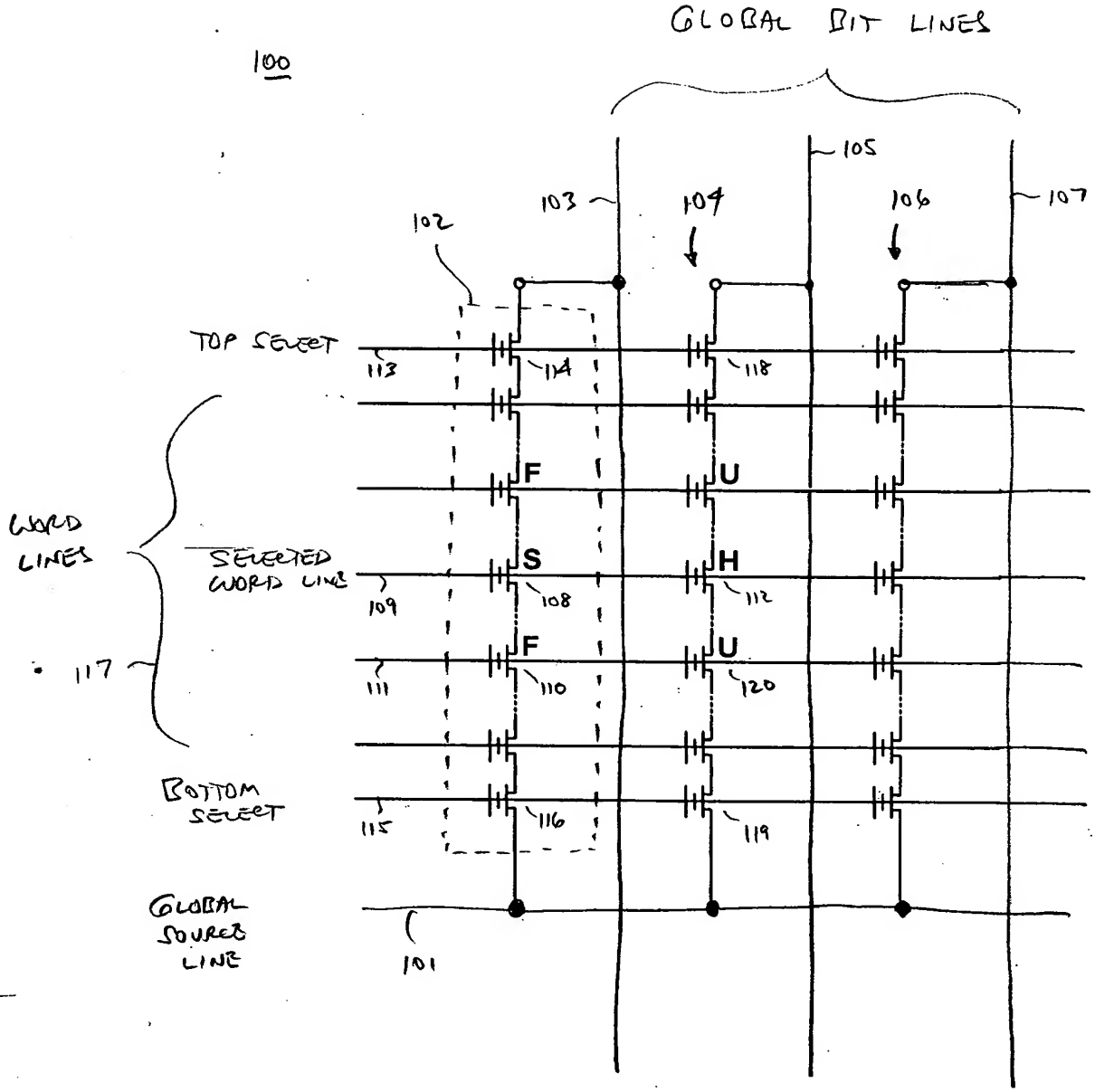

100
GLOBAL BIT LINES
105
103
104
106
107
102
TOP SELECT
113
114
118
WORD LINES
F
U
SELECTED WORD LINE
S
H
109
108
112
117
F
U
111
110
120
BOTTOM SELECT
115
116
119
GLOBAL SOURCE LINE
101

Fig. 1

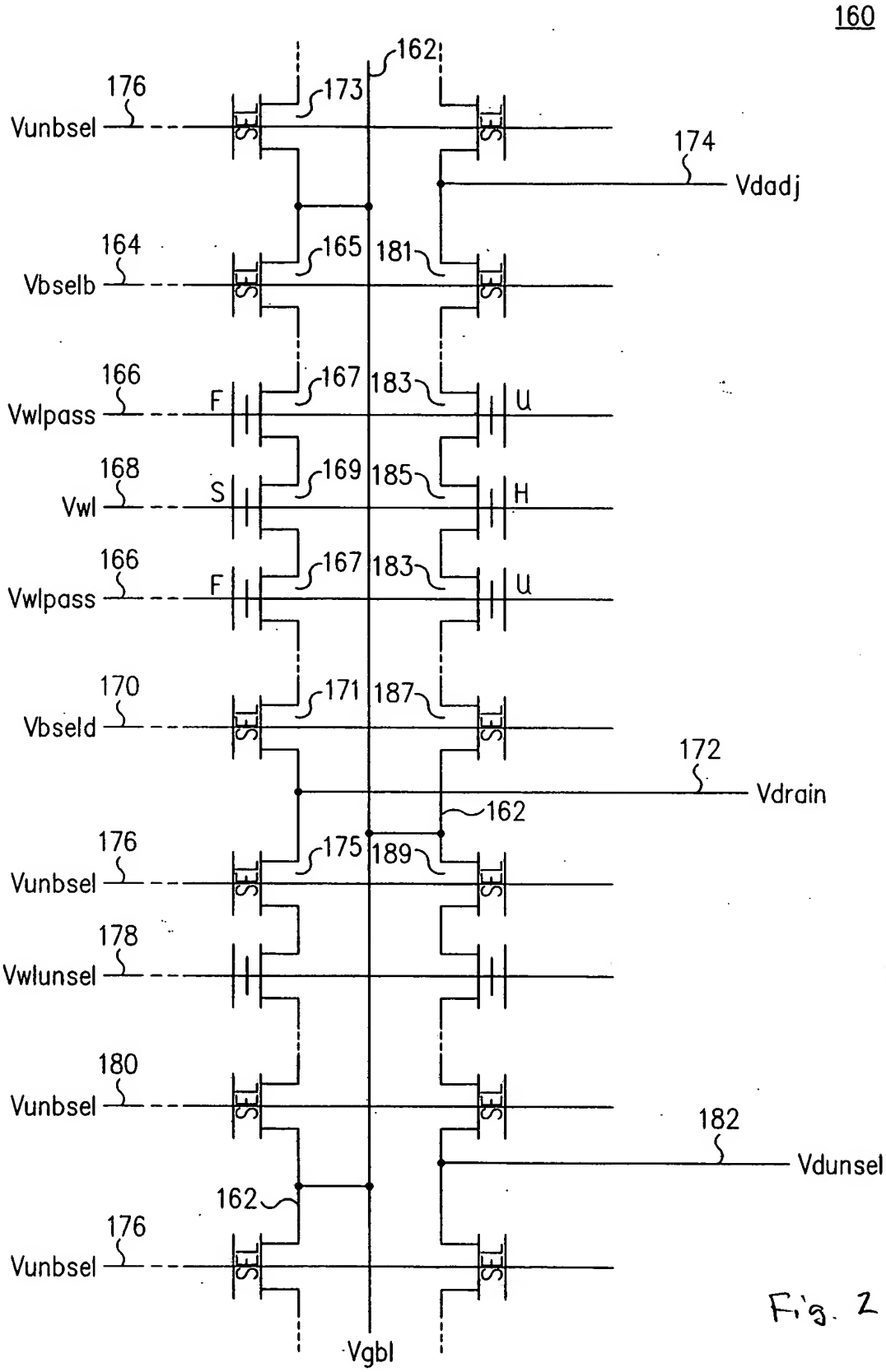

160
162
176
Vunbsel
173
174
Vdadj
164
Vbselb
165
181
166
Vwlpass
F
167
183
U
168
Vwl
S
169
185
H
166
Vwlpass
F
167
183
U
170
Vbseld
171
187
172
Vdrain
162
176
Vunbsel
175
189
178
Vwlunsel
180
Vunbsel
182
Vdunsel
162
176
Vunbsel
SEL
Vgbl

Fig. 2

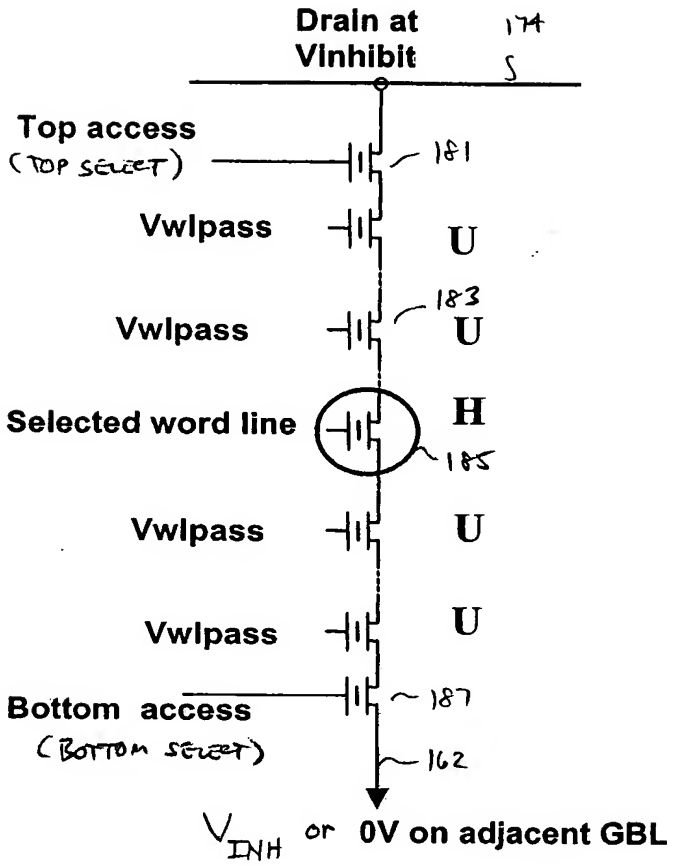

Drain at
Vinhibit
174
S
Top access
(TOP SELECT)
181
Vwlpass
U
183
Vwlpass
U
Selected word line
H
185
Vwlpass
U
Vwlpass
U
Bottom access
(BOTTOM SELECT)
187
162
V_{INH} or 0V on adjacent GBL

Fig. 3

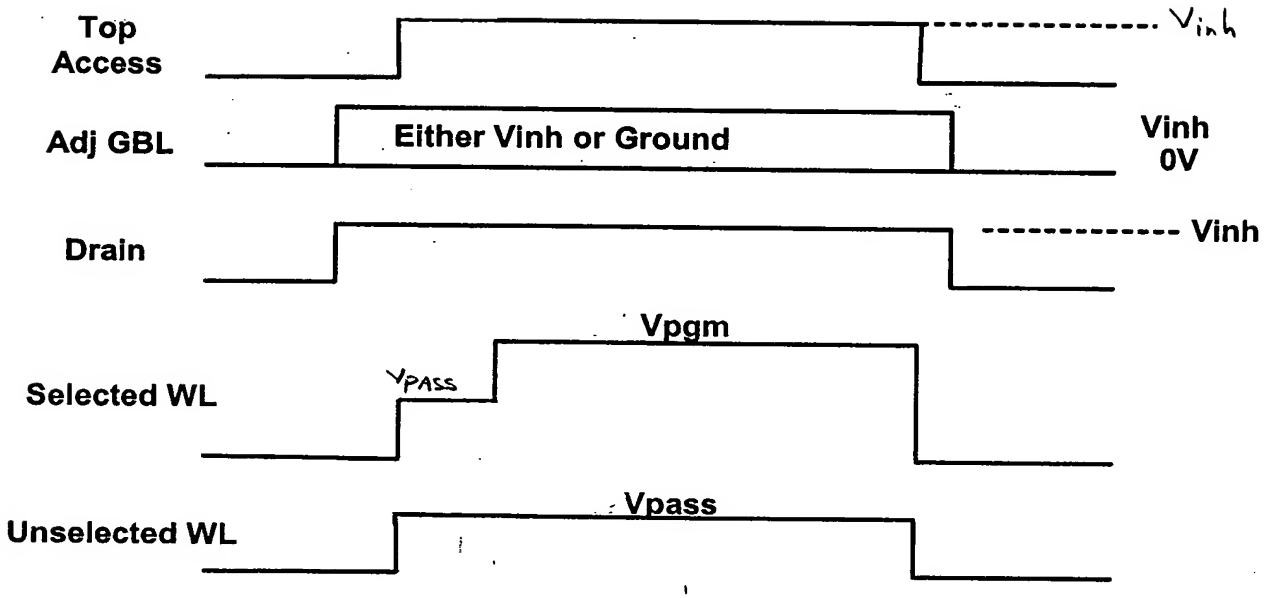

Top Access
Vinh
Adj GBL
Either Vinh or Ground
Vinh
0V
Drain
Vinh
Vpgm
Selected WL
VPASS
Vpass
Unselected WL

Fig. 4

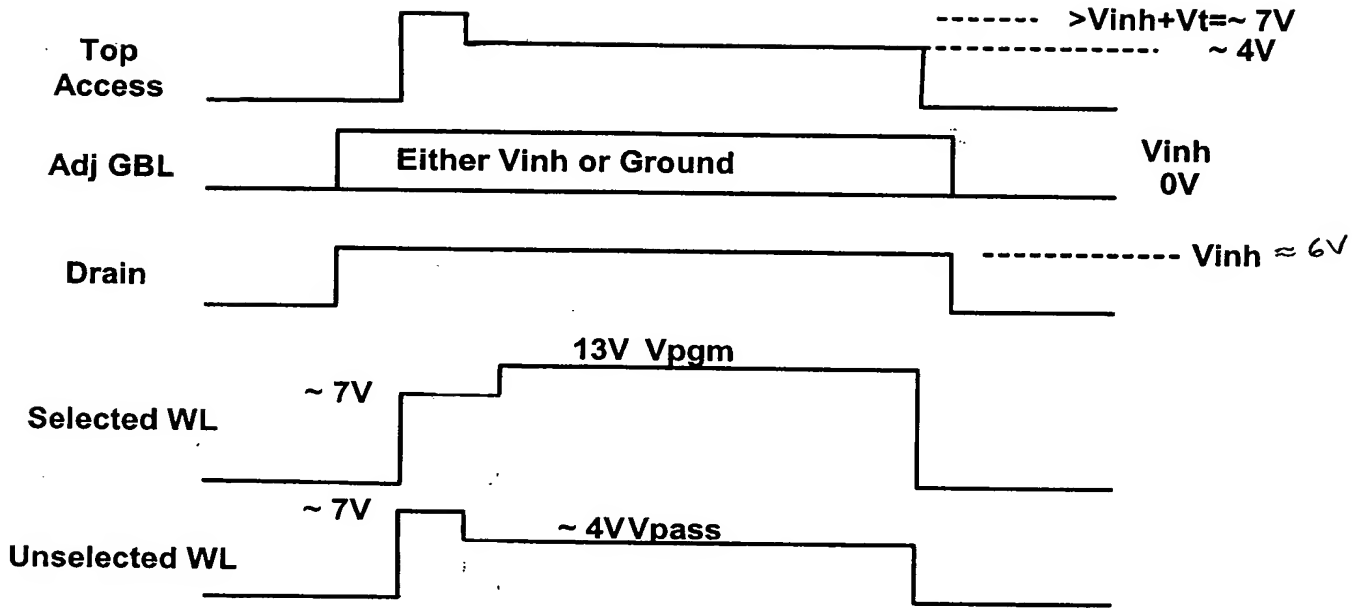

Top Access
>Vinh+Vt=~ 7V
~ 4V
Adj GBL
Either Vinh or Ground
Vinh
0V
Drain
Vinh ≈ 6V
13V Vpgm
~ 7V
Selected WL
~ 7V
~ 4VVpass
Unselected WL

Fig. 5

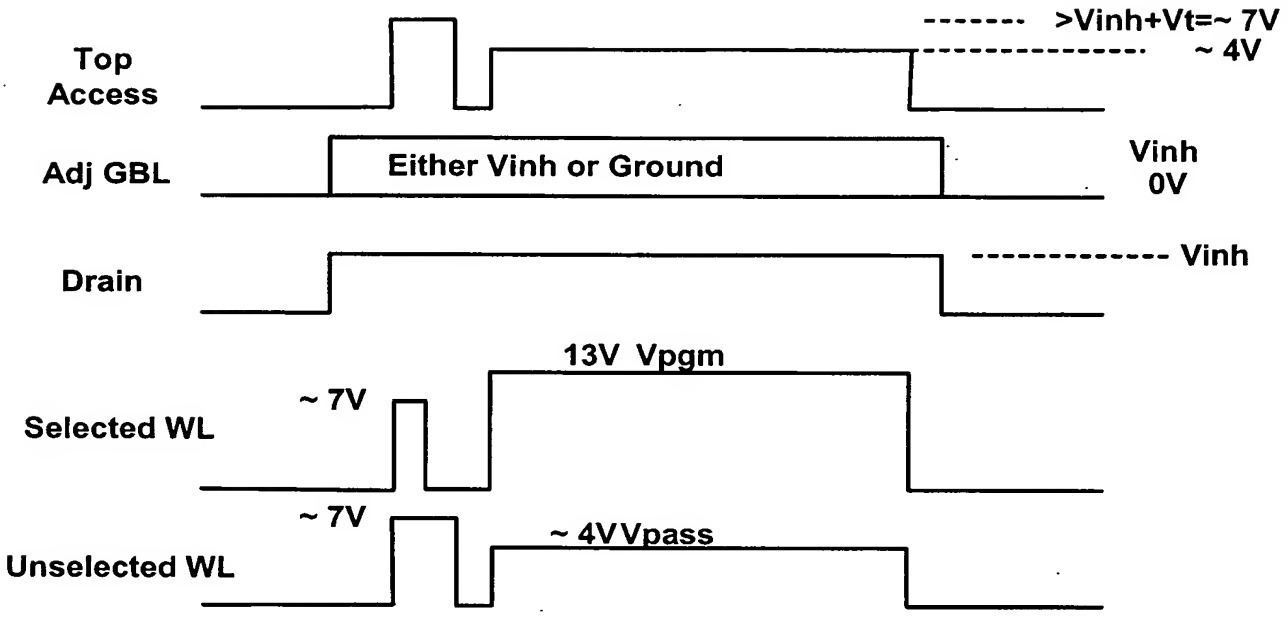

Top
Access
>Vinh+Vt=~ 7V
~ 4V
Adj GBL
Either Vinh or Ground
Vinh
0V
Drain
Vinh
13V Vpgm
~ 7V
Selected WL
~ 7V
~ 4VVpass
Unselected WL

Fig. 6

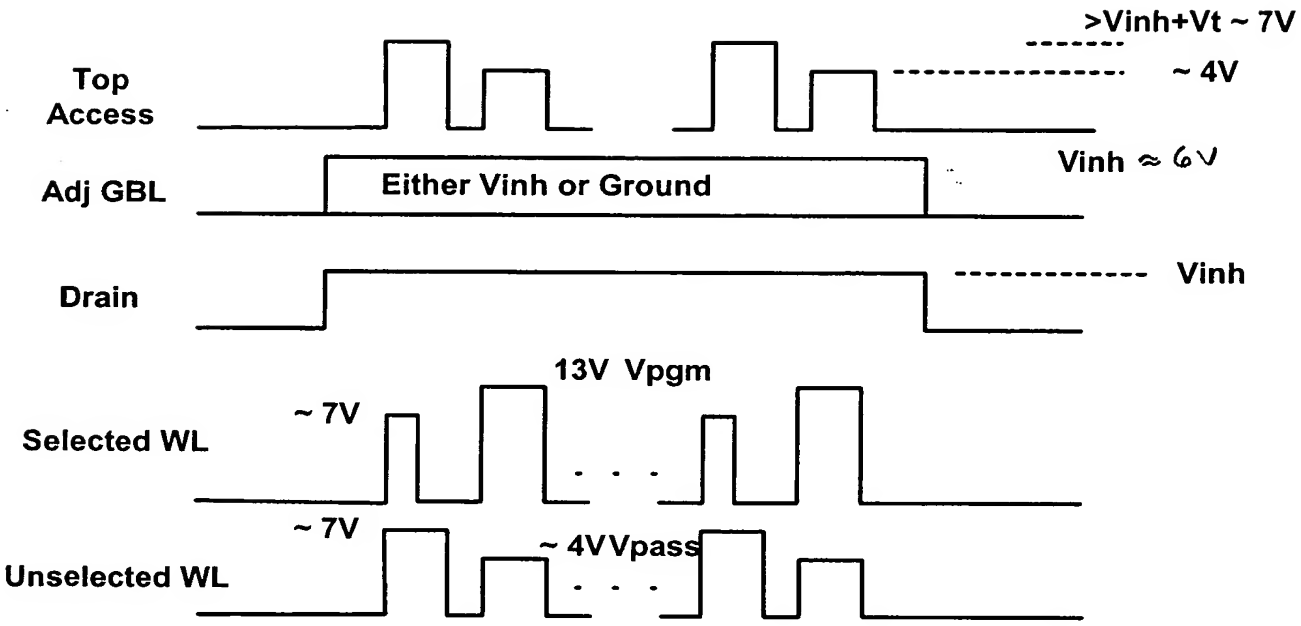
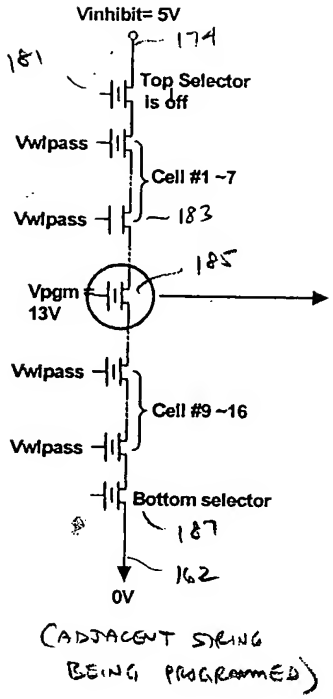

>Vinh+Vt ~ 7V
Top Access
~ 4V
Vinh ≈ 6V
Adj GBL
Either Vinh or Ground
Drain
Vinh
13V Vpgm
~ 7V
Selected WL
~ 7V
~ 4V Vpass
Unselected WL

Fig. 7


Vinhibit= 5V
174
181
Top Selector
Is off
Vwlpass
Cell #1 ~7
Vwlpass
183
185
Vpgm
13V
Vwlpass
Cell #9 ~16
Vwlpass
Bottom selector
187
162
0V
(ADJACENT STRING
BEING PROGRAMED)

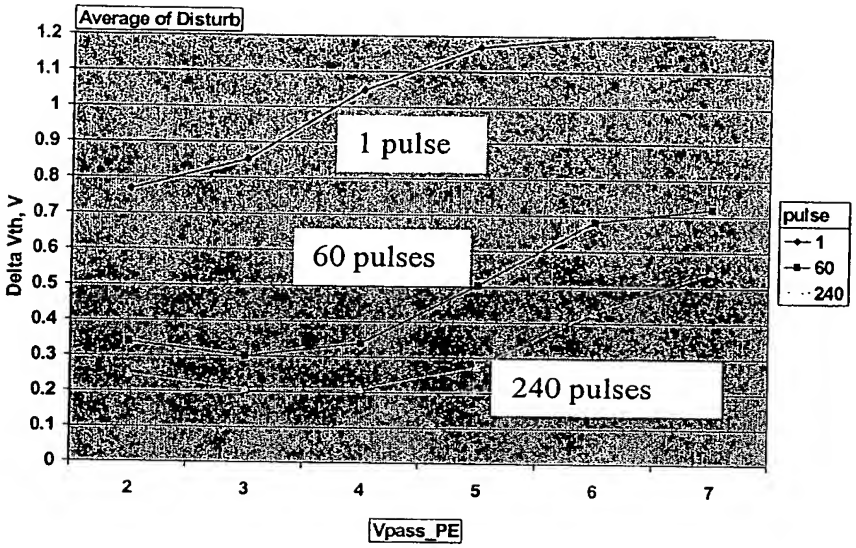

Average of Disturb
Delta Vth, V
1.2
1.1
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
1 pulse
60 pulses
240 pulses
2
3
4
5
6
7
Vpass_PE
pulse
1
60
240

Fig. 8

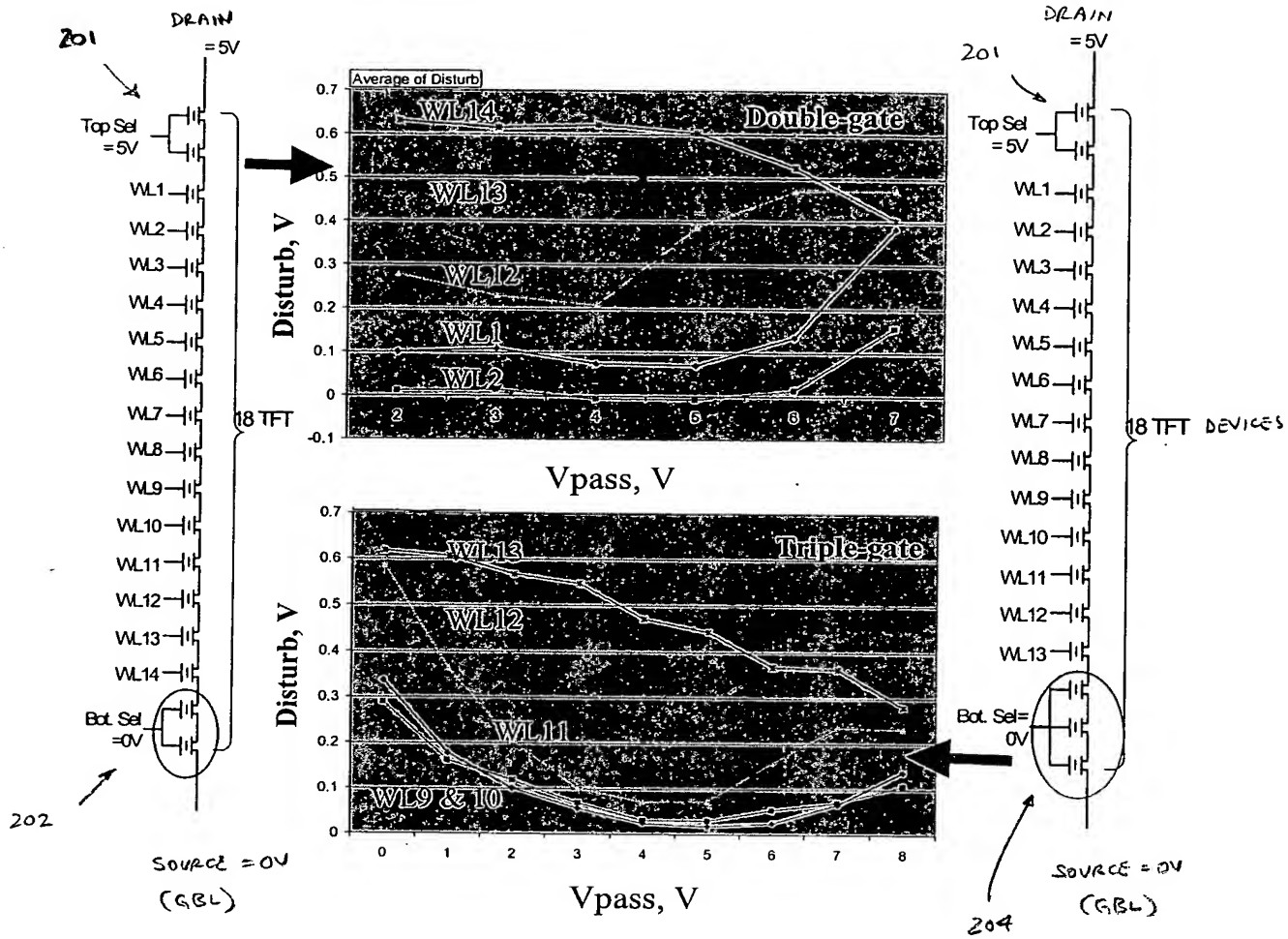

201
DRAIN
=5V
Top Sel
=5V
WL1
WL2
WL3
WL4
WL5
WL6
WL7
WL8
WL9
WL10
WL11
WL12
WL13
WL14
18 TFT
Bot. Sel
=0V
202
SOURCE =0V
(GBL)
Average of Disturb
Double-gate
Disturb, V
Vpass, V
Triple-gate
WL9 &10
201
DRAIN
=5V
Top Sel
=5V
18 TFT DEVICES
Bot. Sel=
0V
204
SOURCE =0V
(GBL)

Fig. 9

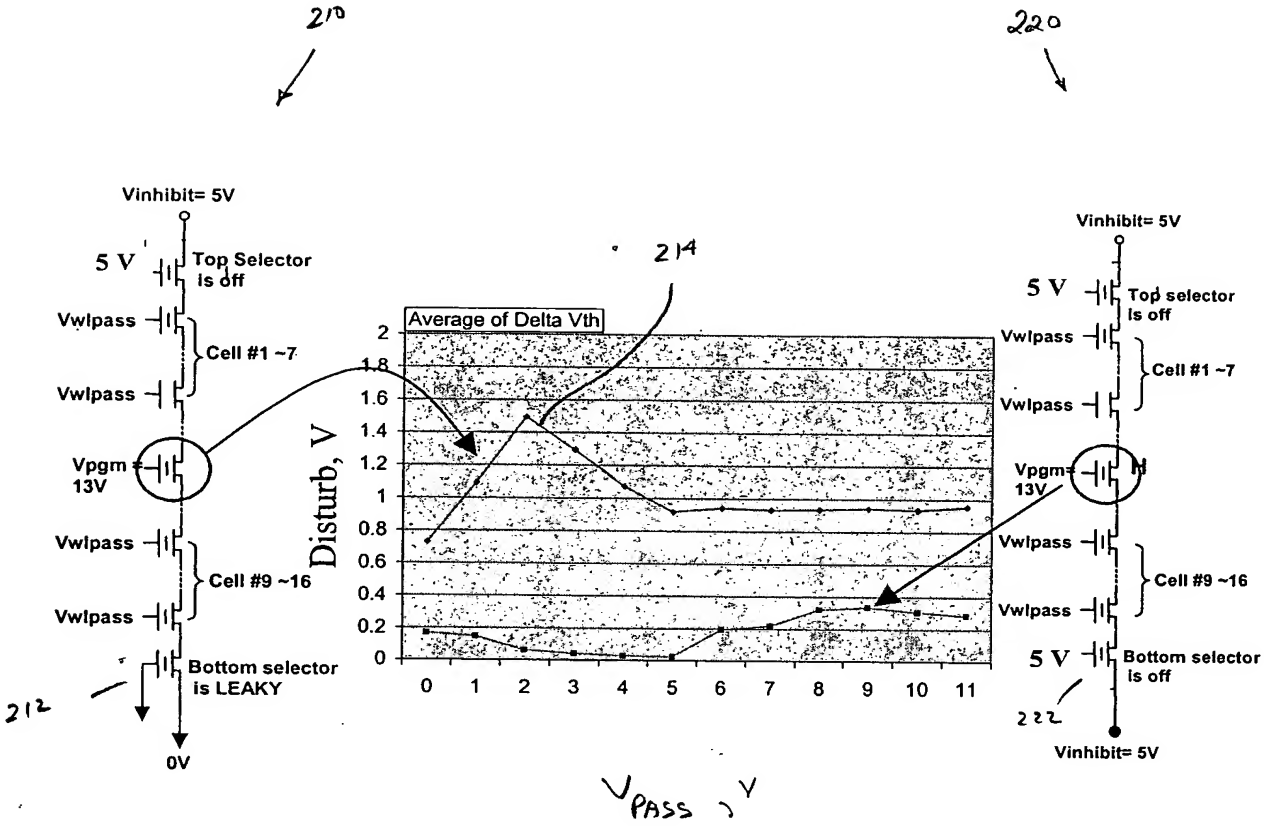
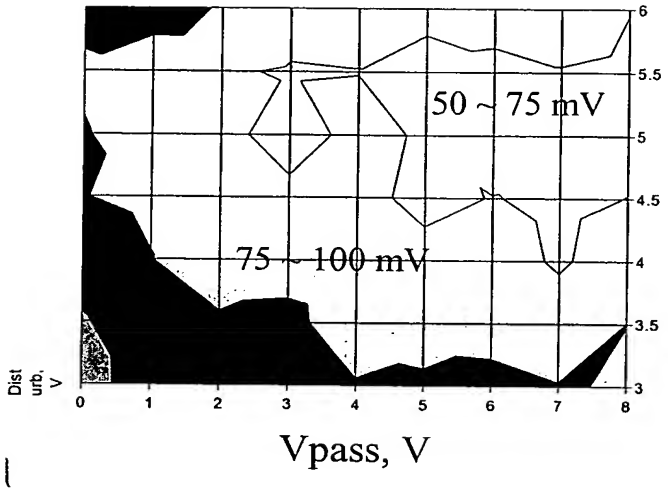

210
220
214
Vinhibit= 5V
5 V
Top Selector is off
Vwlpass
Cell #1 ~7
Vwlpass
Vpgm 13V
Vwlpass
Cell #9 ~16
Vwlpass
Bottom selector is LEAKY
212
0V
Average of Delta Vth
Disturb, V
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0 1 2 3 4 5 6 7 8 9 10 11
VPASS , V
Vinhibit= 5V
5 V
Top selector is off
Vwlpass
Cell #1 ~7
Vwlpass
Vpgm 13V
Vwlpass
Cell #9 ~16
Vwlpass
5 V
Bottom selector is off
222
Vinhibit= 5V

Fig. 10



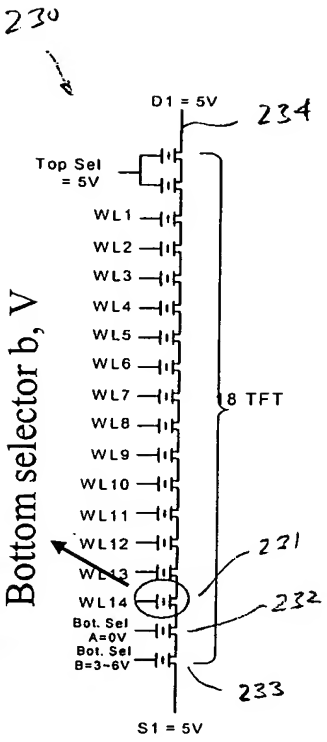
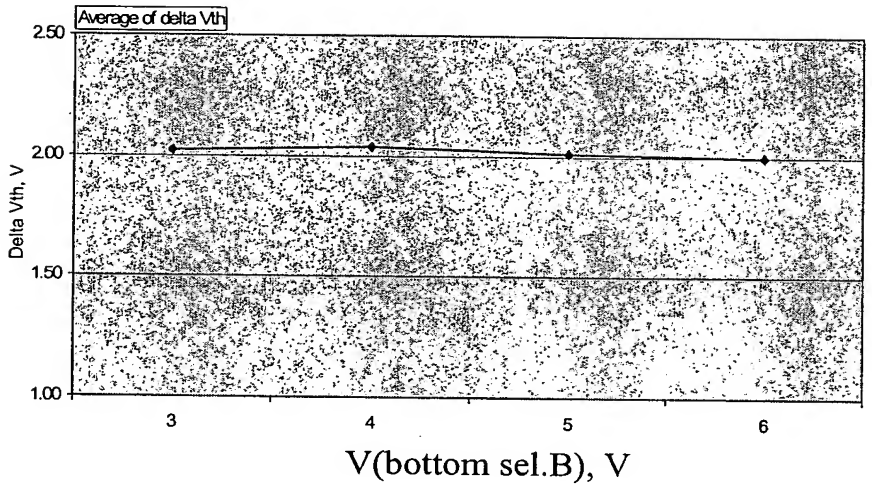


Fig. 11



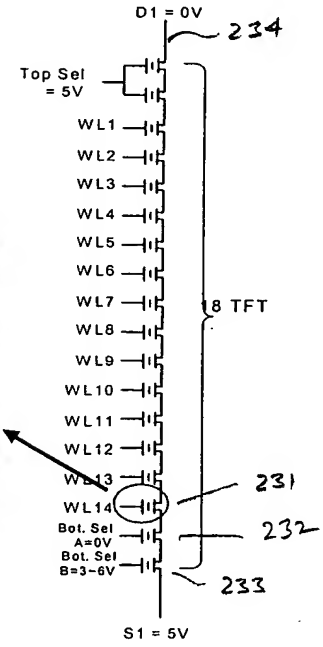


Fig. 12

230

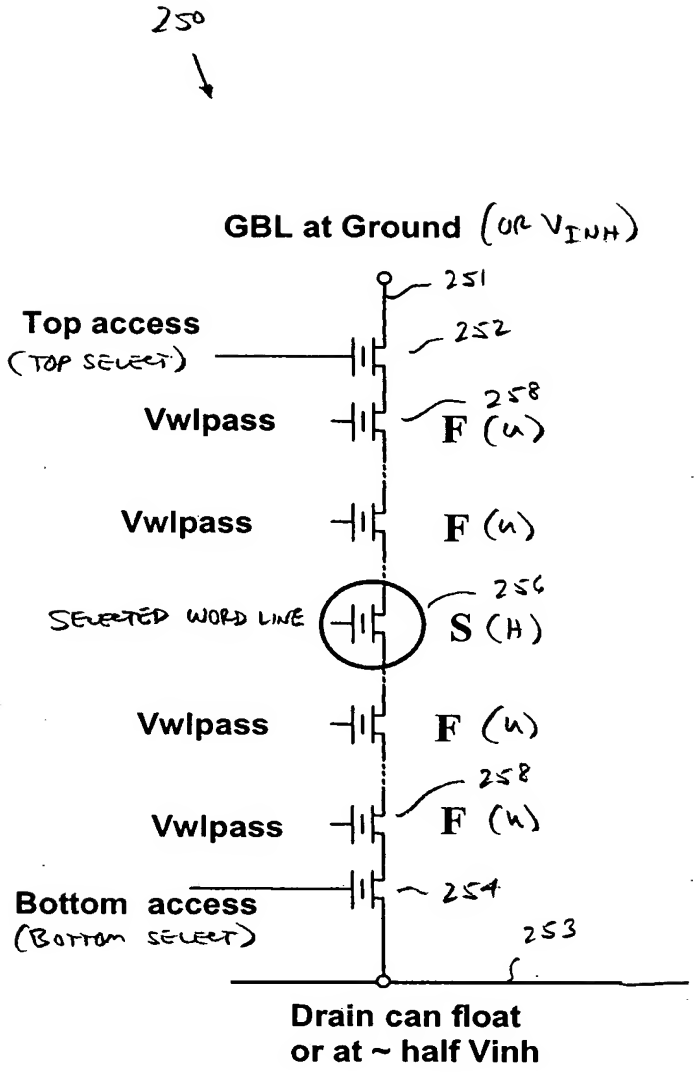

250
GBL at Ground (OR V_{INH})
251
Top access
(TOP SELECT)
252
Vwlpass
258
F (u)
Vwlpass
F (u)
SELECTED WORD LINE
256
S (H)
Vwlpass
F (u)
Vwlpass
258
F (u)
Bottom access
(BOTTOM SELECT)
254
253
Drain can float
or at ~ half Vinh

Fig. 13

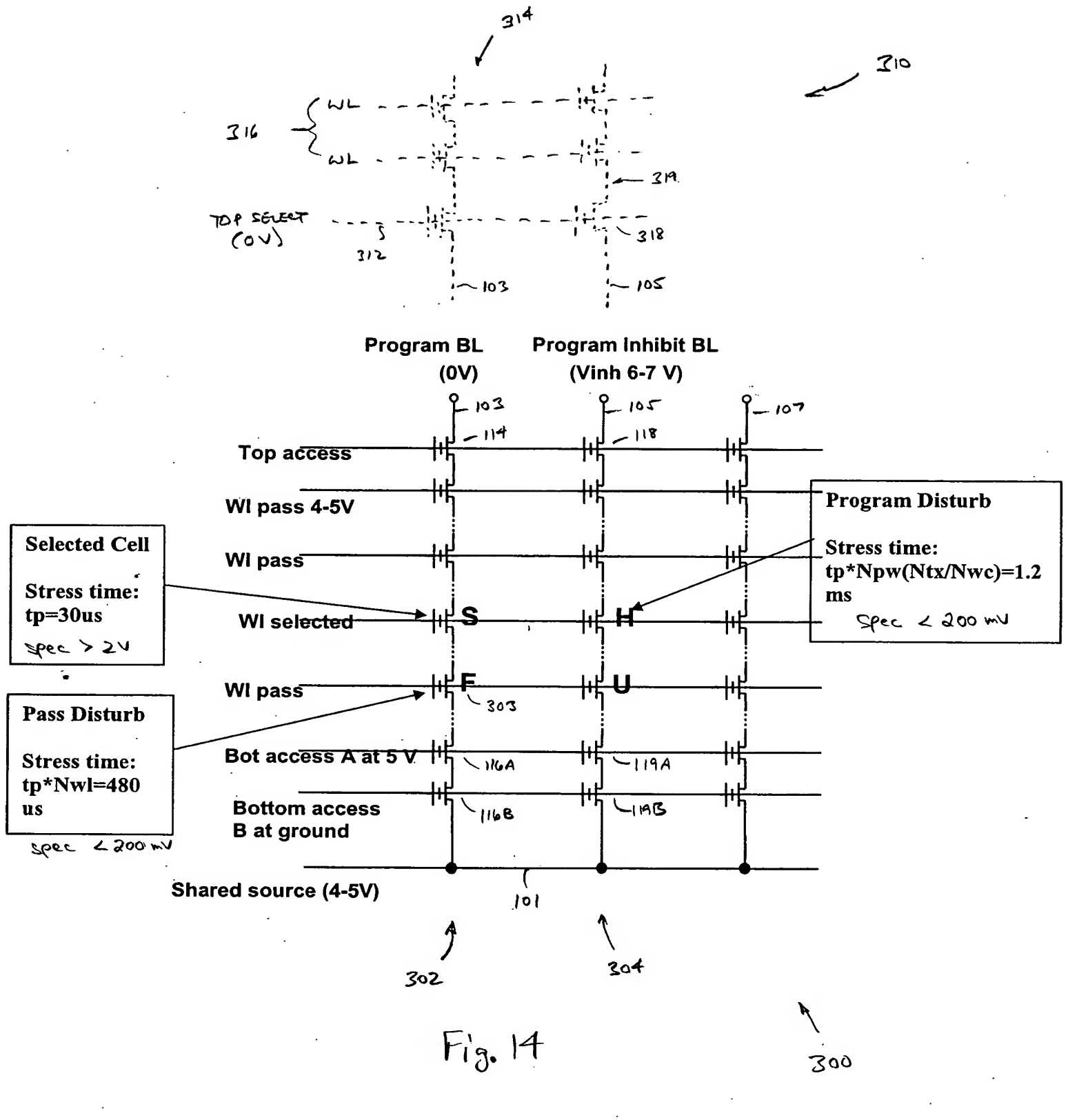

314
310
316
WL
WL
319
TOP SELECT (0V)
312
318
103
105
Program BL (0V)
Program Inhibit BL (Vinh 6-7 V)
103
105
107
114
118
Top access
WI pass 4-5V
WI pass
WI selected
S
H
WI pass
F
U
303
Bot access A at 5 V
116A
119A
Bottom access B at ground
116B
119B
Shared source (4-5V)
101
302
304
300
Selected Cell
Stress time: tp=30us
spec > 2V
Pass Disturb
Stress time: tp*Nwl=480 us
spec < 200 mV
Program Disturb
Stress time: tp*Npw(Ntx/Nwc)=1.2 ms
Spec < 200 mV

Fig. 14

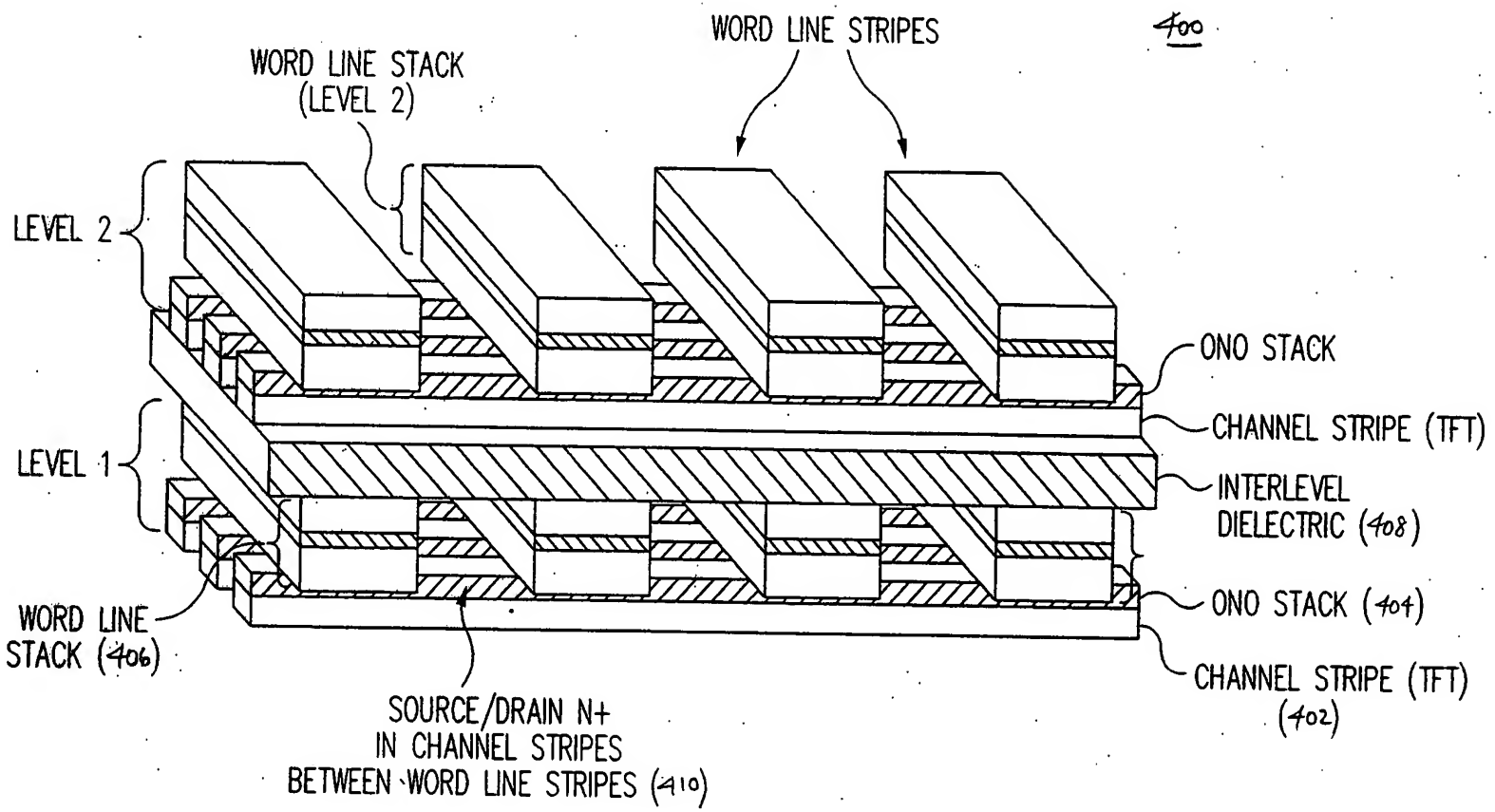

400
WORD LINE STRIPES
WORD LINE STACK
(LEVEL 2)
LEVEL 2
LEVEL 1
ONO STACK
CHANNEL STRIPE (TFT)
INTERLEVEL
DIELECTRIC (408)
ONO STACK (404)
CHANNEL STRIPE (TFT)
(402)
WORD LINE
STACK (406)
SOURCE/DRAIN N+
IN CHANNEL STRIPES
BETWEEN WORD LINE STRIPES (410)

Fig. 15

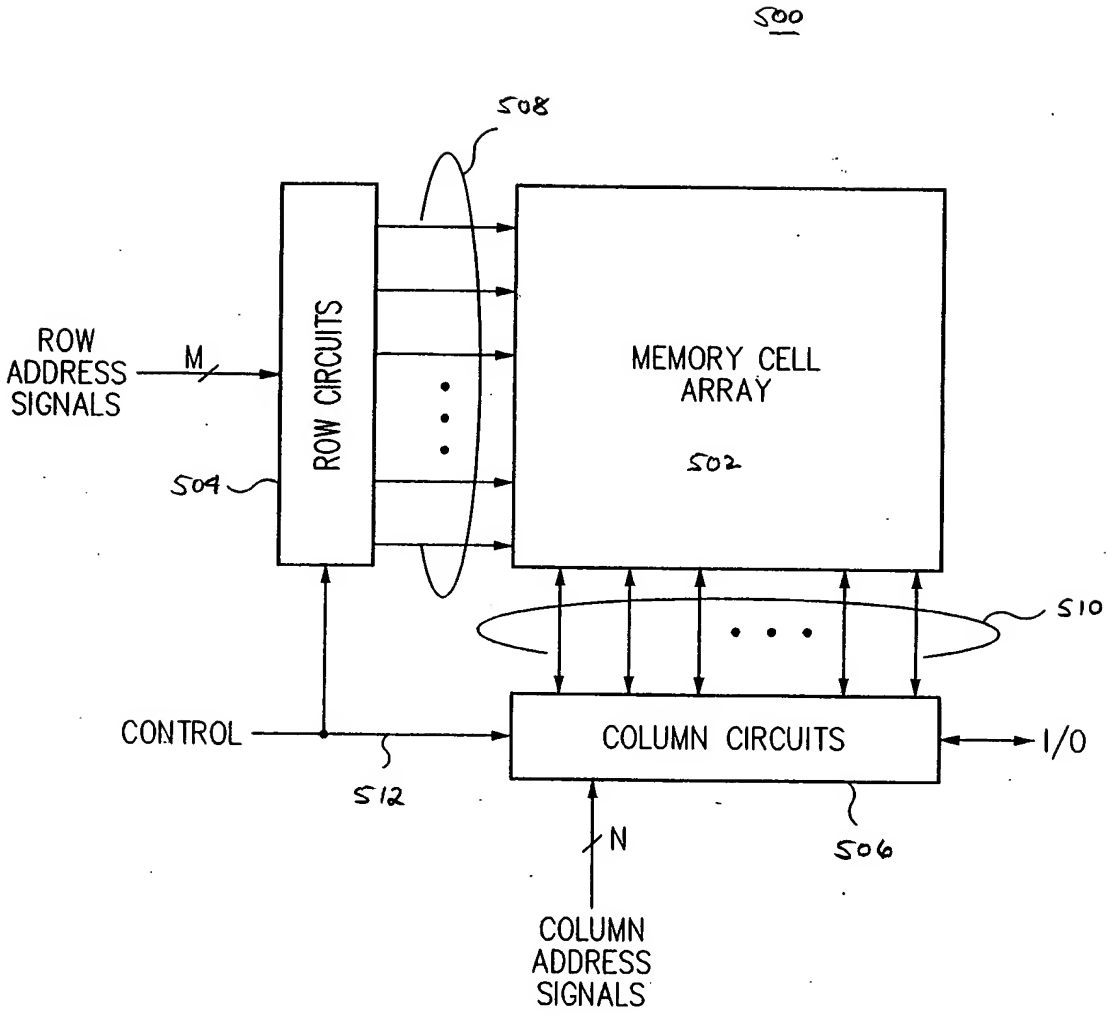
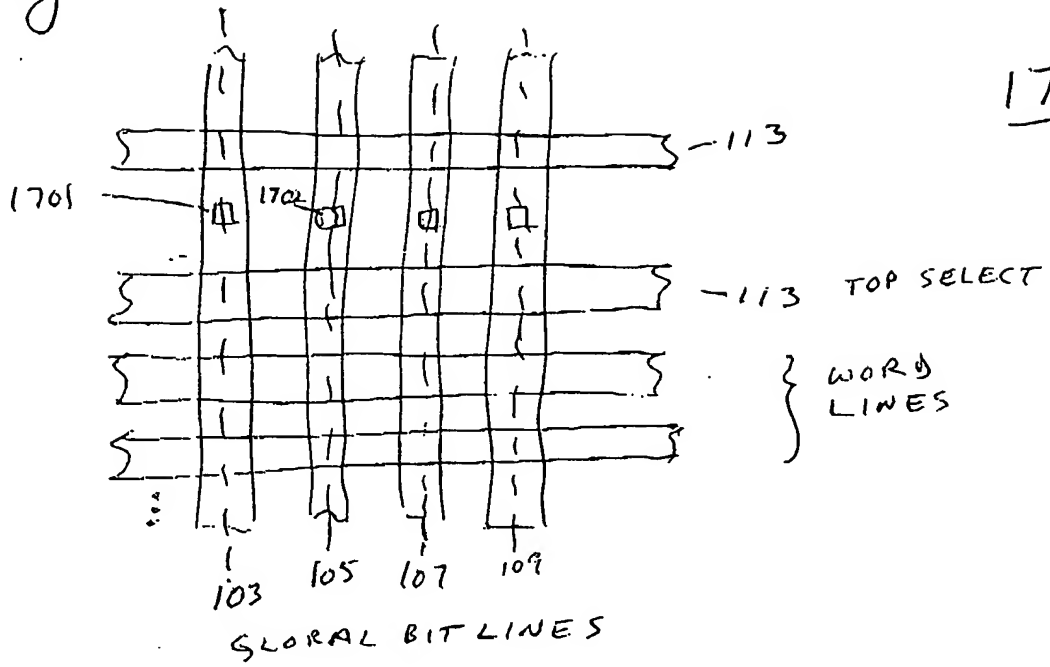

500
508
ROW ADDRESS SIGNALS
M
ROW CIRCUITS
504
MEMORY CELL ARRAY
502
510
CONTROL
512
COLUMN CIRCUITS
I/O
506
N
COLUMN ADDRESS SIGNALS

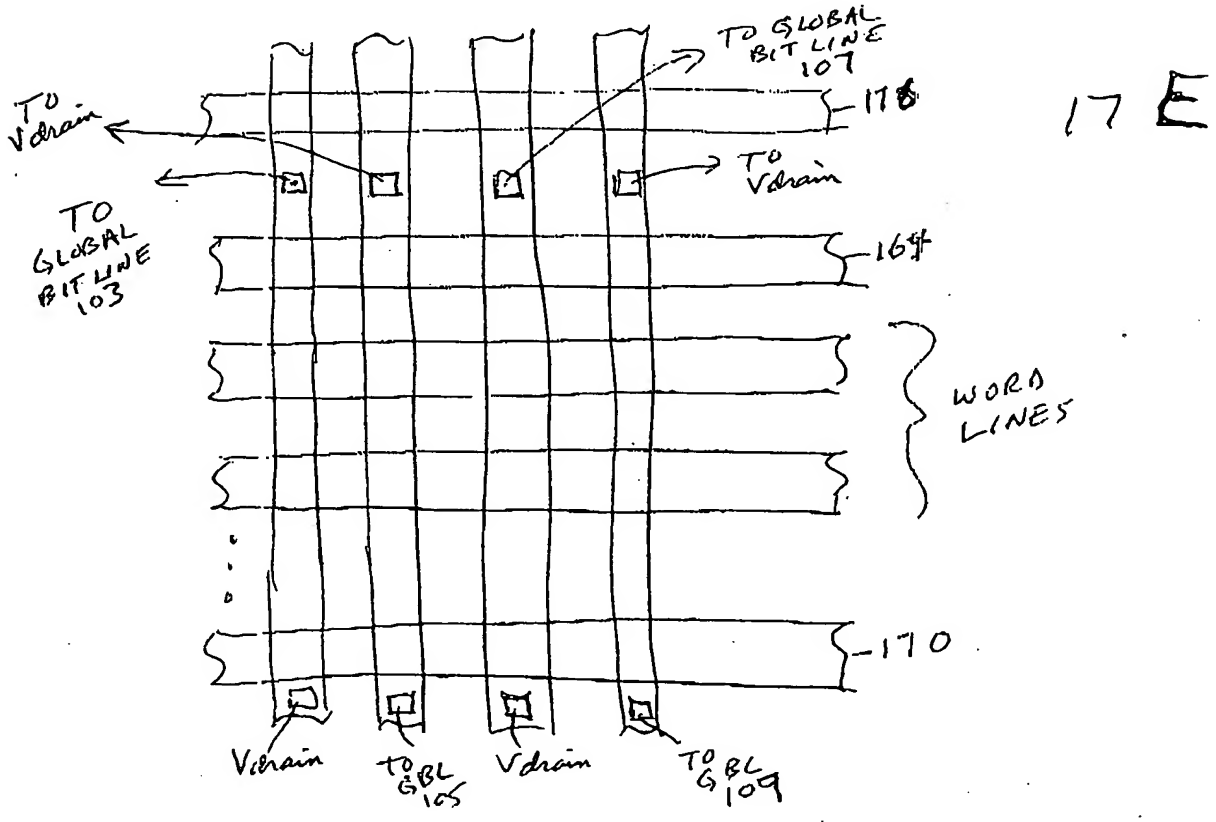
FIG. 16

Fig 17



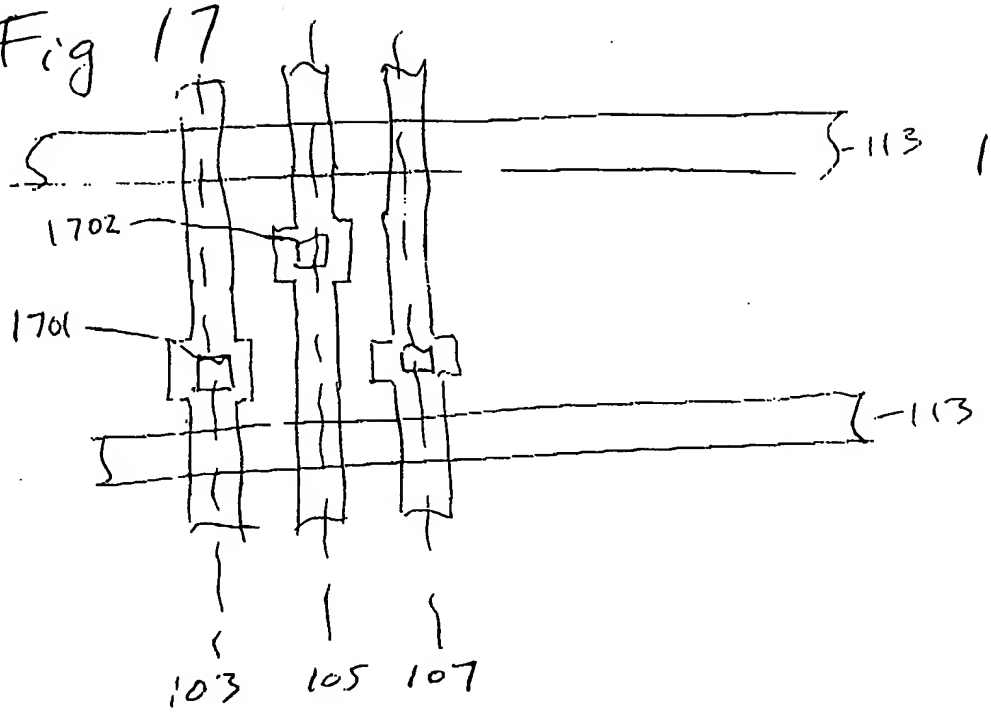
17A

GLOBAL BIT LINES 103, 107 ON ONE LAYER
GLOBAL BIT LINES 105, 109 ON 2ND LAYER
17B

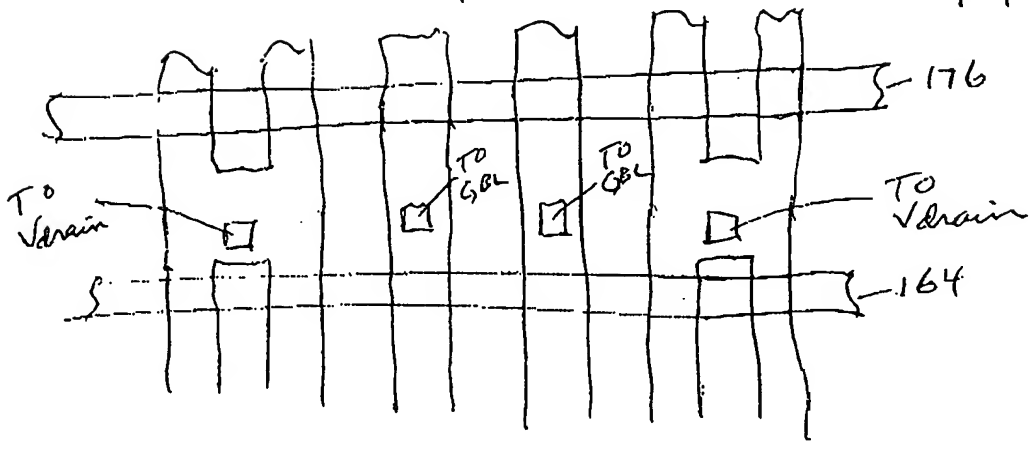


17E

Fig 17



17C



17D

Fig. 18